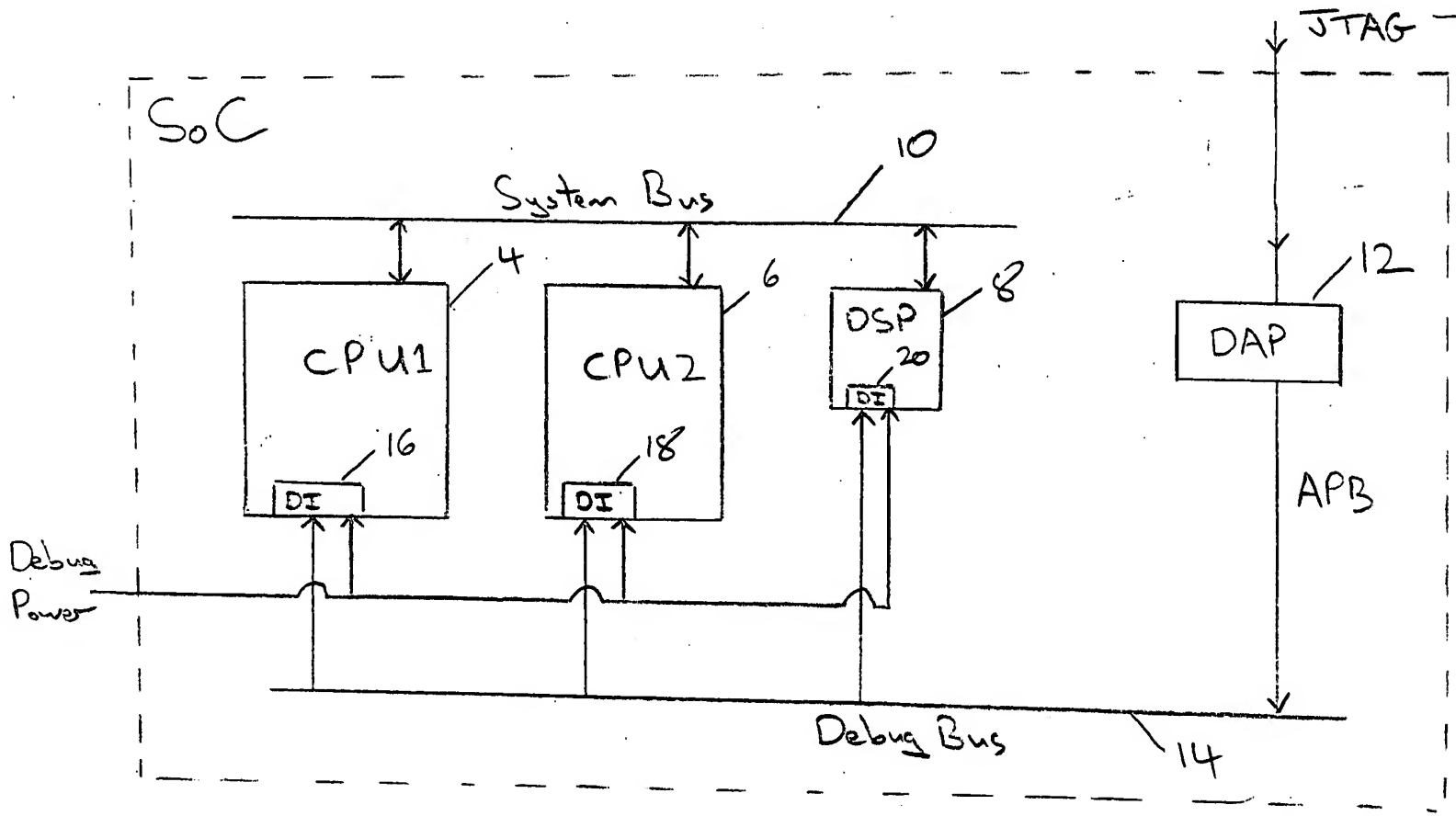

JTAG TAP
SoC
System Bus
10
4
6
8
12
CPU1
CPU2
DSP
DAP
20
DI
16
18
APB
Debug Power
Debug Bus
14

2

Fig. 1

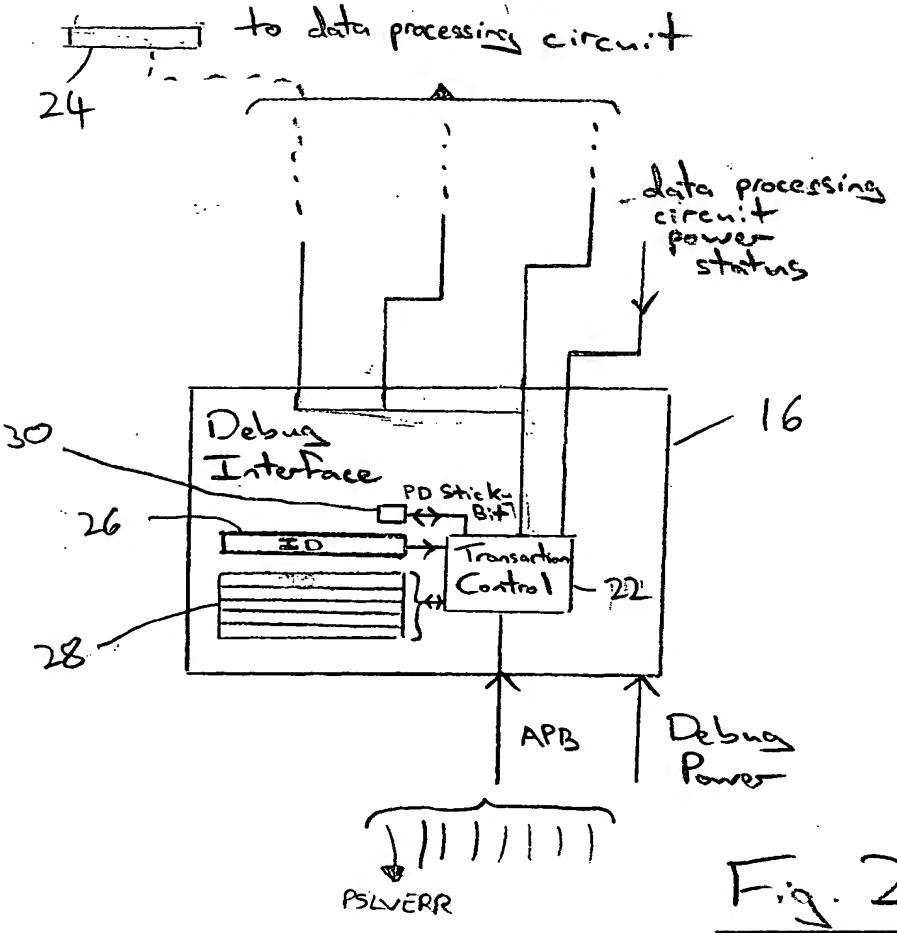
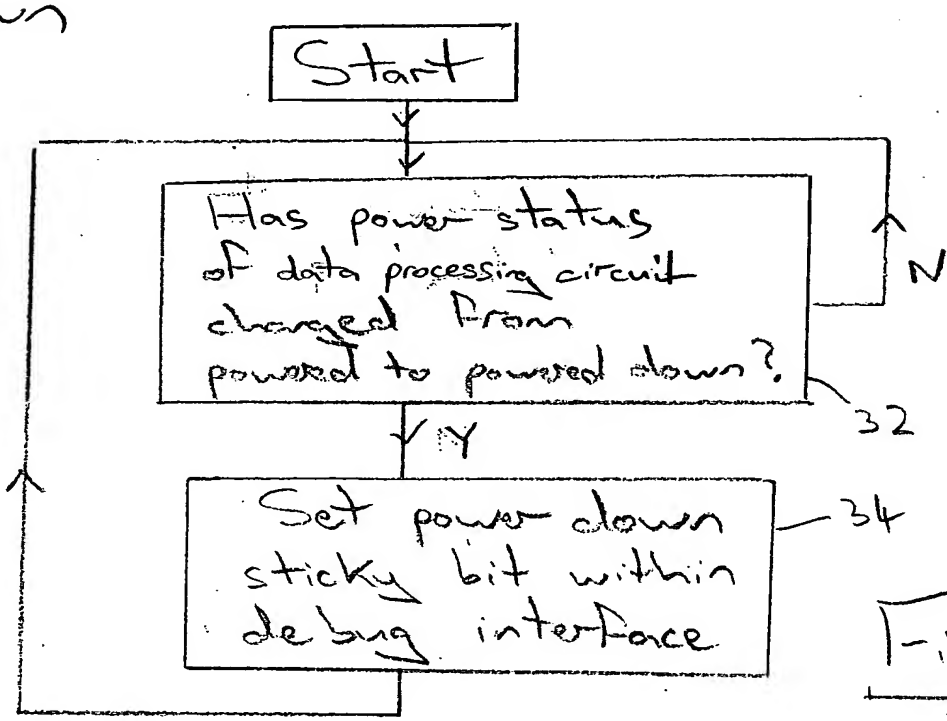


Fig. 2

Power Down Sticky Bit Setting



other edge trig FF.

Fig. 3

Debug Bus Error Generation

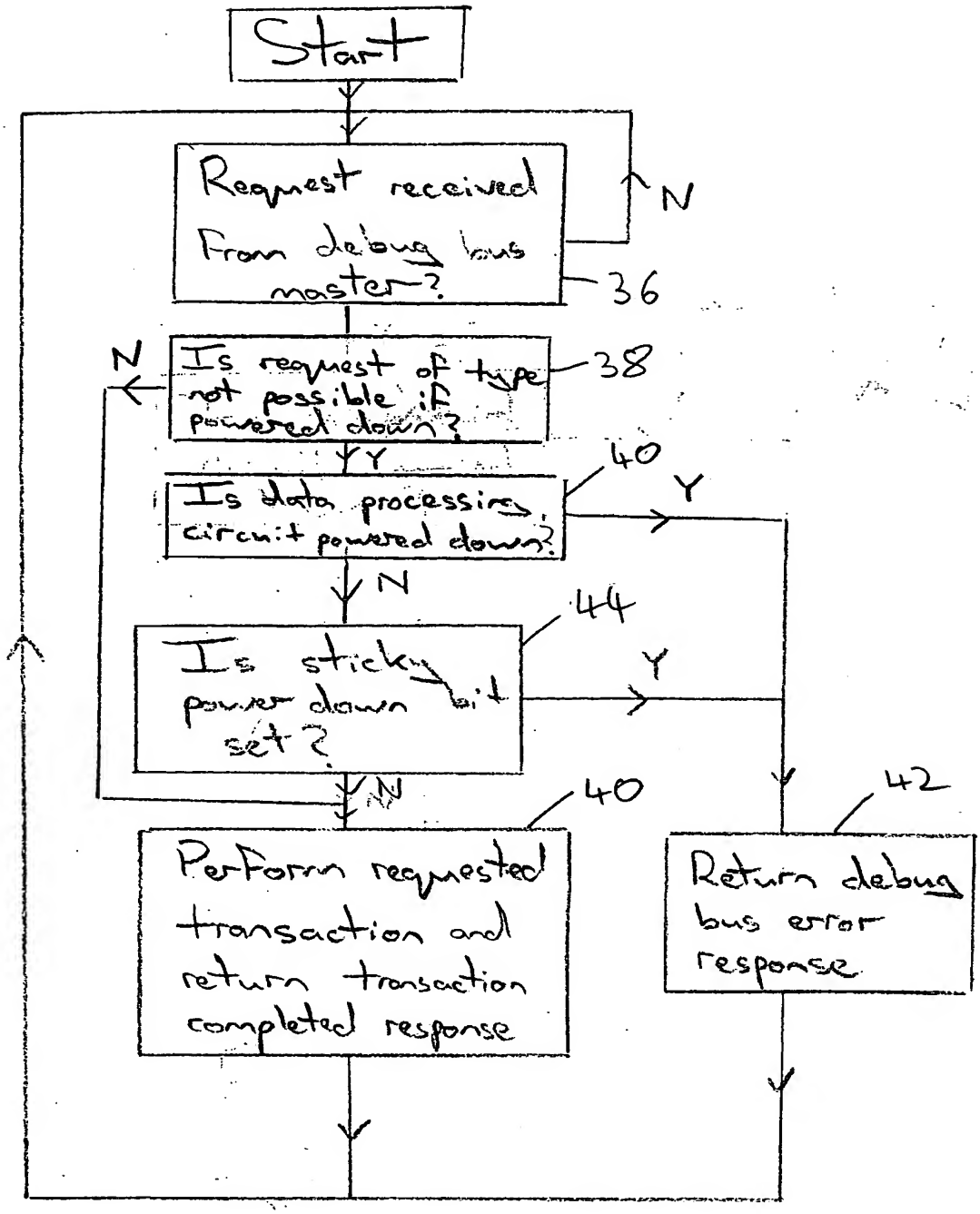


Fig. 4